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PATENT
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Assistant Commissioner for Patents
Washington, D.C. 20231

By: Sherry Barton

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

MO, BRIAN SZE-KI, et al.

Application No.: Not yet assigned

For: METHOD OF FORMING A TRENCH TRANSISTOR HAVING A SUPERIOR GATE DIELECTRIC

Examiner: Not yet assigned

Art Unit: Not yet assigned

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Prior to examination of the above-referenced application, please enter the following amendments and remarks.

IN THE TITLE:

Please amend the title as follows: --METHOD OF FORMING A TRENCH TRANSISTOR HAVING A SUPERIOR GATE DIELECTRIC--.

IN THE SPECIFICATION:

Please insert the following heading and sentence, prior to the heading reading "BACKGROUND OF THE INVENTION" on page 1 of the application:

--CROSS-REFERENCE TO RELATED APPLICATIONS

This is a division of Application No. 09/286,168, filed on April 5, 1999.--

Please amend the paragraph beginning at line 27 on page 2 of the application as follows:

--The present invention provides a trench metal oxide semiconductor field effect transistor (MOSFET) with a rugged gate dielectric layer which exhibits lower gate leakage current. Gate dielectric (e.g. oxide) is grown on the trench walls and bottom at a temperature sufficiently high to reduce the viscosity of the oxide during growth to result in an oxide layer of more uniform thickness. In one embodiment, the high-temperature oxide layer is grown at 1,100°C to a thickness of about 500 Å thick and exhibits reduced gate leakage current and higher gate rupture voltage compared to a trench transistor with a gate oxide layer of similar thickness grown at the lower temperatures (e.g., 950°C) conventionally used in the industry. In a preferred embodiment, a gate dielectric layer is made from a first layer of high-temperature gate oxide, a layer of silicon nitride, and a second layer of gate oxide. This composite gate dielectric layer at optimized thicknesses results in even lower gate leakage current and higher gate rupture voltage.--

Please amend the paragraph beginning at line 18 on page 3 of the application as follows:

-- In another embodiment, the present invention provides a field effect transistor formed on a silicon substrate, the transistor including a trench extending into the substrate, the trench being substantially filled by a conductive material that is

separated from trench walls and bottom by a dielectric material, the dielectric material including: a silicon nitride layer sandwiched between a first oxide layer adjacent to the trench walls and bottom, and a second oxide layer adjacent to the conductive material, the first oxide layer having a thickness that is substantially greater than that of the second oxide layer.--

IN THE CLAIMS:

Please cancel claims 1-8.

REMARKS

Upon entry of this preliminary amendment, which cancels claims 1-8, claims 9-14 remain pending. Applicant requests examination of the pending claims.

CONCLUSION

Applicant believes all claims pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,

William E. Winters
Reg. No. 42,232

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE TITLE:

The title of the patent application has been amended as follows:

--METHOD OF FORMING A TRENCH TRANSISTOR ~~WITH~~ HAVING A SUPERIOR GATE DIELECTRIC--.

IN THE SPECIFICATION:

The paragraph beginning at line 27 on page 2 of the application has been amended as follows:

--The present invention provides a trench metal oxide semiconductor field effect transistor (MOSFET) with a rugged gate dielectric layer which exhibits lower gate leakage current. Gate dielectric (e.g. oxide) is grown on the trench walls and bottom at a temperature sufficiently high to reduce the viscosity of the oxide during growth to result in an oxide layer of more uniform thickness. In one embodiment, the high-temperature oxide layer is grown at 1,100°C to a thickness of about 500 ~~A~~Å thick and exhibits reduced gate leakage current and higher gate rupture voltage compared to a trench transistor with a gate oxide layer of similar thickness grown at the lower temperatures (e.g., 950°C) conventionally used in the industry. In a preferred embodiment, a gate dielectric layer is made from a first layer of high-temperature gate oxide, a layer of silicon nitride, and a second layer of gate oxide. This composite gate dielectric layer at optimized thicknesses results in even lower gate leakage current and higher gate rupture voltage.--

The paragraph beginning at line 18 on page 3 of the application has been amended as follows:

-- In another embodiment, the present invention provides a field effect transistor formed on a silicon substrate, the transistor including a trench extending into the substrate, the trench being substantially filled by a conductive material that is separated from trench walls and bottom by a dielectric material, the dielectric material including: a silicon nitride layer sandwiched between a first oxide layer adjacent to the trench walls and bottom, and a second oxide layer adjacent to the conductive material, the first oxide layer having a thickness that is substantially greater than that of the second oxide layer.--